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NEW SCHEME

Fifth Semester B.E. Degree Examination, Dec. 06 / Jan. 07
Electrical and Electronics Engineering
Operational Amplifier and Linear IC's

Time: 3 hrs.] [Max. Marks:100

Note: ***1. Answer any FIVE full questions.***
2. Missing data may be suitably assumed.
3. Use of Op-amp data sheets is permitted.

1 a. Define the following electrical parameters for an op-amp:
i) Input off-set voltage ii) Input resistance iii) Output voltage swing iv) CMRR. **(08 Marks)**

b. What information does transfer curve reveal about op-amp? **(04 Marks)**

c. Sketch the circuit of a capacitor-coupled voltage follower. Explain the design procedure. **(08 Marks)**

2 a. Define: i) Loop phase shift ii) Loop gain iii) Open-loop-gain iv) Closed loop gain for a feed back system. **(08 Marks)**

b. What is frequency compensation? Explain phase lag or phase lead compensation method. **(08 Marks)**

c. List the precautions that should be observed for op-amp circuit stability. **(04 Marks)**

3 a. The maximum output voltages of each of the voltage comparators shown in fig.3(a) are ±15 V. Sketch the output waveforms for each when V_{in} is a 10 V peak sine wave. In each case show V_{in} and V_o and label voltage levels where switching occurs. **(06 Marks)**

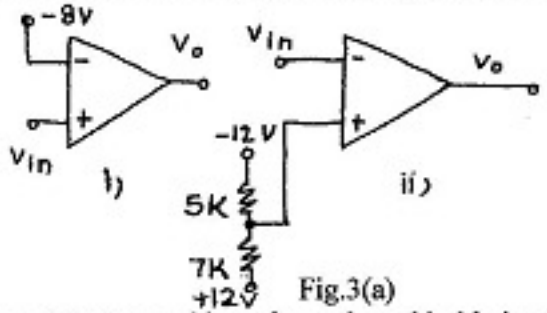

Fig.3(a)

b. Sketch and explain the working of sample and hold circuit. **(06 Marks)**

c. Name the op-amp circuit shown in fig.3(c) and explain its working and sketch its transfer curve. **(08 Marks)**

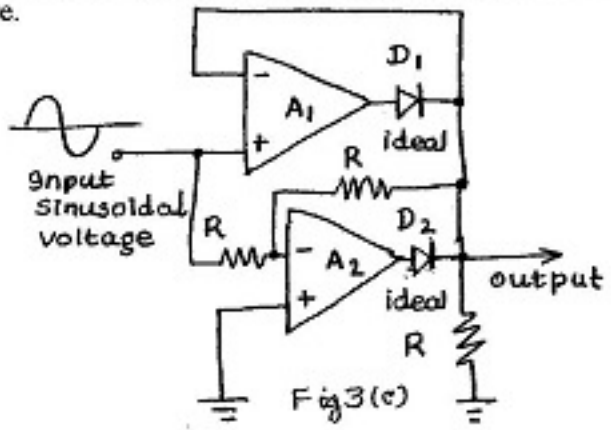

Fig3(c)

Contd.... 2

4 a. Referring to fig.4(a) sketch the output and transfer curve for the given op-amp clipper circuits. Take $V_{in} = 8 \sin\omega t$ volts. **(12 Marks)**

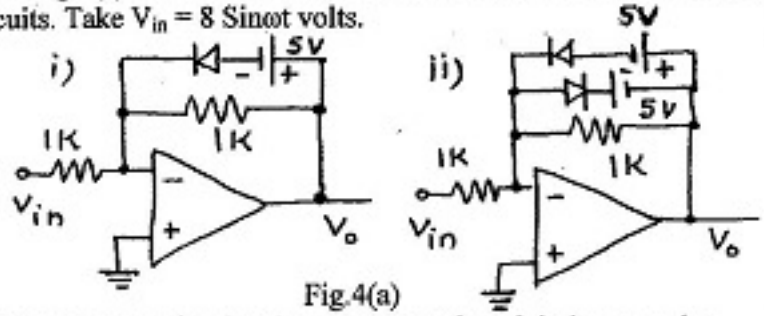

Fig.4(a)

b. Sketch positive clamper circuit using op-amp and explain its operation. **(08 Marks)**

5 a. Sketch the circuitry of an astable multivibrator using op-amp and sketch the relevant waveforms. **(10 Marks)**

b. The output of the Schmitt trigger shown in fig.5(b) switches between +10 V and -10 V.
i) Find the lower and upper trigger levels ii) Find hysterisis iii) Sketch the hysterisis loop iv) Sketch the output when V_{in} is a 10 V peak sine wave. **(10 Marks)**

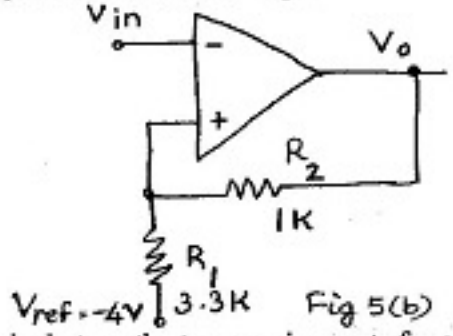

Fig 5(b)

6 a. Define an oscillator and what are the two requirements for oscillation. **(03 Marks)**

b. Sketch Wein Bridge oscillator circuit and derive expression for the:
i) frequency of the waveform generated and ii) gain required for sustaining oscillations. **(12 Marks)**

c. Sketch the output of an integrator shown in fig.6(c) on the graph sheet. Take R_1 = 1 K, C = 0.1 μF. **(05 Marks)**

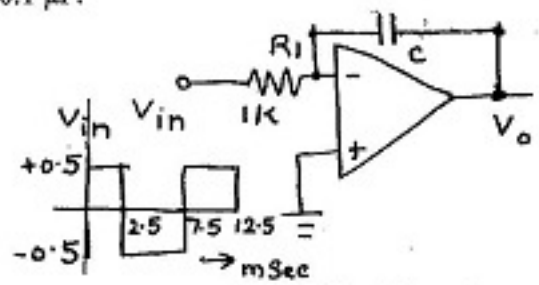

Fig.6(c)

7 a. Derive expression for gain and phase angle of first order low pass Butterworth filter. **(08 Marks)**

b. What is a phase – locked loop? Explain the working of building blocks of PLL. **(08 Marks)**

c. What is a dc voltage regulator? Define: i) line regulation ii) load regulation. **(04 Marks)**

8 a. Sketch the circuit of a voltage follower regulator. Explain its operation. **(06 Marks)**

b. Sketch the basic circuit of 723 voltage regulator and explain the regulator action. **(10 Marks)**

c. Differentiate small signal amplifiers and power amplifiers. **(04 Marks)**

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